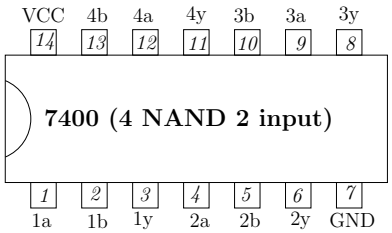
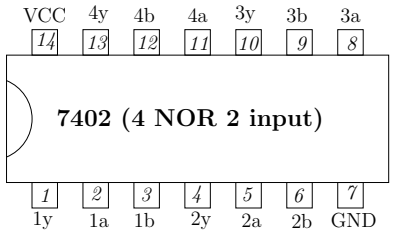
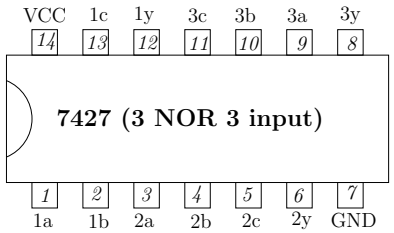
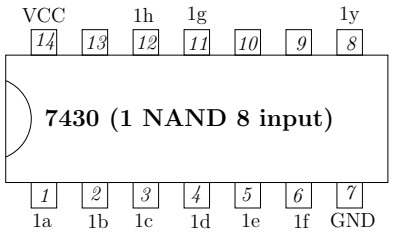
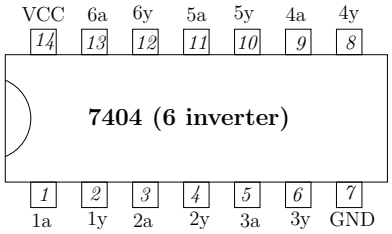
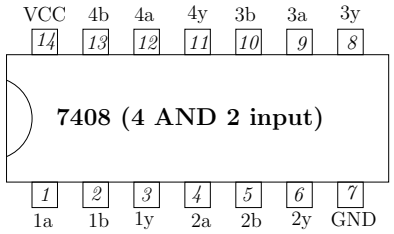

VCC 4b 4a 4y 3b 3a 3y
14 13 12 11 10 9 8
7400 (4 NAND 2 input)
1 2 3 4 5 6 7
1a 1b 1y 2a 2b 2y GND

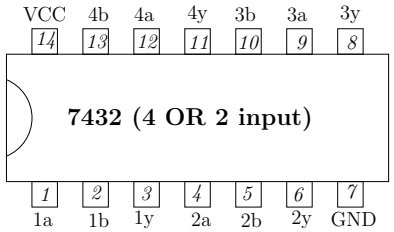

VCC 4y 4b 4a 3y 3b 3a
14 13 12 11 10 9 8
7402 (4 NOR 2 input)
1 2 3 4 5 6 7
1y 1a 1b 2y 2a 2b GND

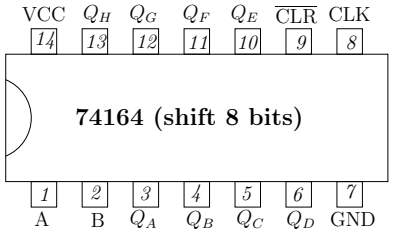

VCC 1c 1y 3c 3b 3a 3y
14 13 12 11 10 9 8
7427 (3 NOR 3 input)
1 2 3 4 5 6 7
1a 1b 2a 2b 2c 2y GND

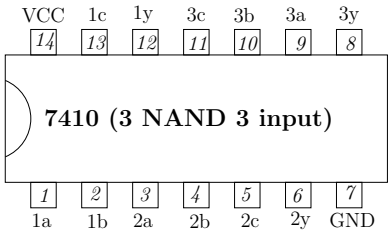

VCC 1h 1g 1y
14 13 12 11 10 9 8
7430 (1 NAND 8 input)
1 2 3 4 5 6 7
1a 1b 1c 1d 1e 1f GND

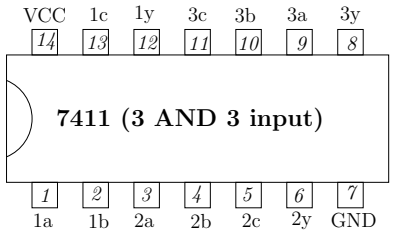

VCC 6a 6y 5a 5y 4a 4y
14 13 12 11 10 9 8
7404 (6 inverter)
1 2 3 4 5 6 7
1a 1y 2a 2y 3a 3y GND

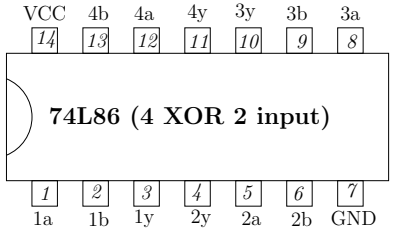

VCC 4b 4a 4y 3b 3a 3y
14 13 12 11 10 9 8
7408 (4 AND 2 input)
1 2 3 4 5 6 7
1a 1b 1y 2a 2b 2y GND

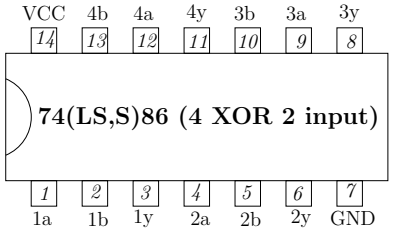

VCC 4b 4a 4y 3b 3a 3y
14 13 12 11 10 9 8
7432 (4 OR 2 input)
1 2 3 4 5 6 7
1a 1b 1y 2a 2b 2y GND

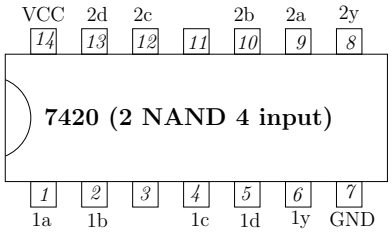

VCC Q_H Q_G Q_F Q_E $\overline{\text{CLR}}$ CLK
14 13 12 11 10 9 8
74164 (shift 8 bits)
1 2 3 4 5 6 7
A B Q_A Q_B Q_C Q_D GND

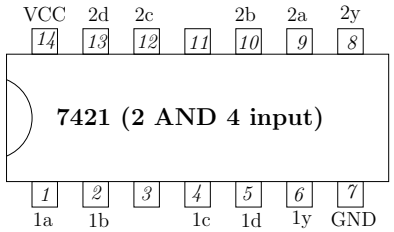

VCC 1c 1y 3c 3b 3a 3y
14 13 12 11 10 9 8
7410 (3 NAND 3 input)
1 2 3 4 5 6 7
1a 1b 2a 2b 2c 2y GND

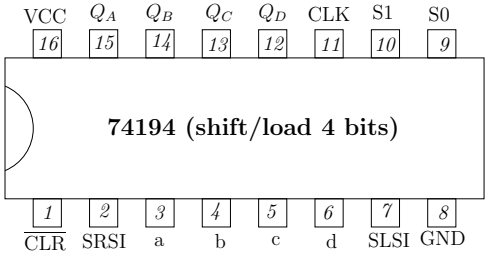

VCC 1c 1y 3c 3b 3a 3y
14 13 12 11 10 9 8
7411 (3 AND 3 input)
1 2 3 4 5 6 7
1a 1b 2a 2b 2c 2y GND


VCC 4b 4a 4y 3y 3b 3a
14 13 12 11 10 9 8
74L86 (4 XOR 2 input)
1 2 3 4 5 6 7
1a 1b 1y 2y 2a 2b GND


VCC 4b 4a 4y 3b 3a 3y
14 13 12 11 10 9 8
74(LS,S)86 (4 XOR 2 input)
1 2 3 4 5 6 7
1a 1b 1y 2a 2b 2y GND


VCC 2d 2c 2b 2a 2y
14 13 12 11 10 9 8
7420 (2 NAND 4 input)
1 2 3 4 5 6 7
1a 1b 1c 1d 1y GND


VCC 2d 2c 2b 2a 2y
14 13 12 11 10 9 8
7421 (2 AND 4 input)
1 2 3 4 5 6 7
1a 1b 1c 1d 1y GND


VCC Q_A Q_B Q_C Q_D CLK S1 S0
16 15 14 13 12 11 10 9
74194 (shift/load 4 bits)
1 2 3 4 5 6 7 8
$\overline{\text{CLR}}$ SRSI a b c d SLSI GND